REMARKS

Claims 1-16, 41-50, and 66-85 are pending in the current application, and claims 1, 6, 9, 13-14, 41, 44, 47-48, 66-68, 71-76, and 78-82 have been amended. **If the Examiner does not allow all of the claims after considering this Response, the undersigned requests that the Examiner contact him to schedule and conduct a telephone interview before issuing a subsequent Office Action.**

Specification Objection

The specification is amended herein. Applicants' Attorney submits that the specification is allowable and respectfully requests withdrawal of this objection.

Claim Objection

Claim 1 was objected to because of the hyphen in the term 'hardwired-pipeline circuit.' The term 'hardwired-pipeline' is a compound adjective in this context, and therefore the use of a hyphen is grammatically correct. (*See e.g.,* The Elements of Style, 3rd ed., Strunk & White, 1979, p34-35). Applicants' Attorney therefore requests withdrawal of this objection.

Rejection of Claims 1-6, 9-12, 15-16, 41-42, 44-46, 49-50, 66, 73, 76-77, and 80 under 35 U.S.C. § 112 ¶1

Examiner indicates that he fails to understand how a pipeline can be indicated without generating some form of 'virtual' address.

Devices or hardware components can be identified via virtual or non-virtual addresses. Virtual addresses reference a non-physical entity and the referenced non-physical entity then references a physical address (*e.g.*, in a look-up table). On the other hand, a physical or non-virtual address directly references a physical location, device or component.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [94] – [102] of the patent application, in an embodiment, a hardwired-pipeline circuit 80 is operable to process data with an indicated processing pipeline 74 without first using a virtual

address corresponding to the indicated processing pipeline 74. Here, only physical addresses or identifiers are used. The pipeline unit address (*i.e.,* a physical address of a pipeline unit 78) and instance identifier for one of a plurality of pipelines (*e.g.*, pipeline 74_1) described in paragraph [97] are both physical addresses or identifiers and do not correspond to a physical location in a lookup-table. Likewise, the pointer described in paragraph [98] is also a physical address.

In contrast, for example, referring to Figs. 1 and 4 and col. 6, lines 9-35 of Inagaki (U.S. 7,177,310), a physical address table 106 or look-up table is required to create correspondence between virtual addresses and physical addresses (*i.e.,* virtual and non-virtual MAC addresses). Here, a physical address lookup unit 105 extracts a destination IP address163 from an IP packet 134 and refers to a physical address table 106 to identify a virtual address that the IP packet 134 should be sent to. A packet data controller 102 then transmits IP packets to the virtual MAC address and not to the physical MAC address.

Accordingly, the present patent application enables indication of a pipeline without using a virtual address. Therefore claims 1-6, 9-12, 15-16, 41-42, 44-46, 49-50, 66, 73, 76-77, and 80 are in condition for allowance.

Rejection Of Claim 1-12, 15-16, 41-46, 49-50, 66, 69-70, 73, 76-77, 80, and 83 Under 35 U.S.C. § 103(a) As Being Unpatentable Over U.S. 7,177,310 to Inagaki In View Of The Examiner's Taking Of Official Notice

Claim 1

Claim 1 as amended recites a hardwired pipeline circuit operable, without executing a program instruction, to process data with an indicated processing pipeline without first using a virtual address corresponding to the indicated processing pipeline.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [94] – [102] of the patent application, in an embodiment, a hardwired-pipeline circuit 80 is operable to process data with an indicated processing pipeline 74 without first using a virtual address (see, *e.g.*, paragraph [98]) corresponding to the indicated processing pipeline 74. An input-data handler 120 dissects a message that may have a data payload (*i.e.,*

data to be processed by a pipeline 74); a pipeline unit address (*e.g.*, physical address for pipeline unit 78, which comprises pipelines $74_1 - 74_n$); and a pipeline identifier (*e.g.*, an identifier of one of pipelines $74_1 - 74_n$). The data payload is written to a location in DPSRAM 100. A pointer to this location of the data payload and an indication of a destination pipeline (*i.e.,* one of pipelines $74_1 - 74_n$) is stored in an input data queue 112. This pipeline indicator relates to a physical address of a pipeline and not a virtual address. When the selected pipeline is ready to process the data payload, the pointer to the data payload location is sent to the selected pipeline, and the selected pipeline retrieves and processes the data payload.

In contrast, Inagaki does not disclose or suggest processing data with a pipeline without first using a virtual address corresponding to the pipeline. Referring to FIG. 1 and col. 5, line 66 – col. 6, line 35 of Inagaki, a module 6 includes functional accelerators 11 – 14, which are assigned respective virtual MAC addresses b – e. The module 6 receives an IP packet 134 having a destination IP address 163 (FIG. 3), a unit 105 extracts the destination IP address, and, in response to the extracted IP address, a table 106 provides the virtual MAC address (*e.g.*, address b) of the functional accelerator (*e.g.*, functional accelerator b 11) for processing the data in the IP packet 134. The IP packet 134 (in the form of an Ethernet frame 130) and the virtual MAC address (*e.g.*, address b) are provided to a section 112, which stores the IP packet 134 in the one of the RAMs 150 – 154 (*e.g.*, RAM_b 151) that corresponds to the virtual MAC address (*e.g.*, address b). Subsequently, the module 6 transfers the IP packet 134 from the RAM (*e.g.*, the RAM_b 151) to the one of the function accelerators 11 – 14 (*e.g.*, function accelerator b 11) having the virtual MAC address (*e.g.*, address b) to which the RAM (*e.g.*, the RAM_b 151) corresponds. Consequently, Inagaki's module 6 cannot function as described if it does not use a virtual MAC address to route the IP packet 134 to the appropriate function accelerator 11 – 14. In fact, per page 36 of the Office Action, Examiner actually agrees that Inagaki uses an IP address to lookup a virtual address before processing data.

Additionally, Applicants' attorney again objects to Examiner's reliance on his Official Notice (*e.g.,* ". . . anything performed in software can be performed solely by

hardware and vice-versa") for this and the other rejections in the Office Action as improper because the substance of the Official Notice is conclusion, not fact. Under the Examiner's premise, no apparatus that performs in hardware what was previously performed in software can ever be patentable.

Examiner is reminded that when an Applicant challenges a factual assertion as not properly officially noticed or not properly based upon common knowledge, the Office must support the finding with adequate documentary evidence in the next Office Action if the rejection is to be maintained. (MPEP §2144.03(C)). The present Office Action fails to provide such documentary evidence.

Additionally, proper use of Official Notice requires compliance with several obligations expressly set forth in the *Manual of Patent Examining Procedure*. The Office Action has failed to meet these obligations. Specifically, the Office has failed to satisfy its obligations under *MPEP* § 2144.03. For example, *MPEP § 2144.03 (B)* expressly requires the Office to provide specific factual findings predicated on sound technical and scientific reasoning to support taking Official Notice. The *MPEP* goes on to explain that this means that the Office should present an Applicant with the explicit basis on which Official Notice is based so that the Applicant is able to challenge the assertion in the next reply after the Office action. (*MPEP §2144.03(B)*). Naked assertions about what is allegedly known in the art, like those made at page 5 of the Office Action, cannot satisfy these requirements.

Furthermore, Inagaki fails to disclose or suggest a hardwired pipeline circuit operable without executing a program instruction. For example, referring to Fig. 1 and col. 4, line 67 and col. 5, lines 1-2, Inagaki teaches "a memory 10 for storing . . . a function accelerator_b to a function accelerator_e (11 to 14)." These functional accelerators are, therefore, embodied in software, and, therefore, can only operate by executing program instructions. Also, Inagaki's claim 11 recites "a found unique address accelerator is implemented by a software."

In response to this latter argument, the examiner states the following on page 5 of the Office Action: "[h]owever, it should be noted that Inagaki makes not a single mention of executing instructions to perform the claimed steps. Hence, it is unclear as to whether Inagaki executes instructions to perform the claimed steps."

First, as discussed above, the examiner is incorrect that "Inagaki makes not a single mention of executing instructions to perform the claimed steps."

But even assuming that the examiner is correct on this point, even the examiner admits that "it is unclear as to whether Inagaki executes instructions to perform the claimed steps." Therefore, Examiner fails to establish a *prima facie* case of obviousness, because even according to the examiner, it is unclear whether or not Inagaki discloses a hardwired pipeline circuit operable, without executing a program instruction, to process data as recited in claim 1. Furthermore, if Inagaki is unclear as to the claim limitation that the examiner is trying to show, then the examiner's taking of Official Notice cannot clarify Inagaki.

Claims 2-5

These claims are patentable at least by virtue of their dependencies from claim 1.

Claim 6

Claim 6 as amended recites a hardwired-pipeline circuit operable without executing a program instruction and operable to process data with an identified destination pipeline without first referencing a virtual address corresponding to the identified destination pipeline.

In contrast, Inagaki does not disclose or suggest processing data with a pipeline without first referencing a virtual address corresponding to the pipeline, nor does Inagaki disclose or suggest a hardwired-pipeline circuit operable without executing a program instruction. These teaching deficiencies are illustrated in the discussion above relating to claim 1.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 7

Claim 7 recites a hardwired-pipeline circuit operable without executing a program instruction and operable to receive data without receiving, with the data, information corresponding to a post-processing destination of the data.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [94] – [102] of the patent application, in an embodiment, a pipeline circuit 80 (FIG. 4) is operable to receive data without receiving information corresponding to the post-processing destination of the data, and yet nonetheless identify a post-processing destination after processing. After data is processed, a communication shell 84 loads a data identifier that identifies or allows for future identification destination peer(s). (see paragraphs [101] and [102]). Such identification of a post-processing location is not based on information corresponding to a post-processing destination received with data.

In contrast, Inagaki does not disclose or suggest a circuit operable to receive data without receiving, with the data, information corresponding to a post-processing destination of the data.

Referring to FIGS. 1 and 3 and columns 6 and 7, Inagaki's module 6 receives an IP packet 134 that includes a destination IP address 163, which corresponds to a post-processing destination of the packet (*e.g.*, col. 7, lines 19-32). The destination IP address 163 stays with the packet IP 134 throughout the packet's journey through the module 6 (*e.g.*, col. 7, lines 19-21). If the module 6 did not receive the destination IP address 163 with the IP packet 134, then the module would be unable to route the processed packet 134 to its proper external destination because the module would not "know" where to send the processed packet.

On page 37 of the Office Action, Examiner argues that information pertaining to a routing module to which the processed data is to be transmitted is not obtained until after data processing. Examiner points to col. 7, lines 14-32 of Inagaki, which teaches using the destination IP address to look-up a destination in a route information table 104. Here, the IP address nonetheless corresponds to a post-processing destination of the data, even if the IP address corresponds to a destination in a route information table, and even if the identification of a destination is made after processing. Inagaki therefore fails to disclose or suggest a circuit operable to receive

data without receiving, with the data, information corresponding to a post-processing destination of the data.

Additionally, Inagaki fails to disclose or suggest a hardwired-pipeline circuit operable without executing a program instruction. This teaching deficiency is illustrated in the discussion above relating to claim 1.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claims 69-70

These claims are patentable at least by virtue of their dependencies from claim 7.

Claim 8

Claim 8 recites a hardwired-pipeline circuit without executing a program instruction and operable to receive data without receiving, with the data, information corresponding to a post-processing destination of the data.

In contrast, Inagaki does not disclose or suggest a circuit operable to receive data without receiving, with the data, information corresponding to a post-processing destination of the data, nor does Inagaki disclose or suggest a hardwired-pipeline circuit operable without executing a program instruction. These teaching deficiencies are illustrated in the discussion above relating to claims 1 and 7.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 9

Claim 9 as amended recites an input-data handler operable to load data into a memory without first retrieving a virtual address corresponding to a specified hardwired pipeline and recites a hardwired pipeline operable without executing a program instruction to process data.

In contrast, Inagaki does not disclose or suggest an input-data handler operable to load data into a memory without first retrieving a virtual address

corresponding to a specified hardwired pipeline. As discussed above in support of the patentability of claim 1, Inagaki's module 6 does not load data into one of the RAMs 150 – 154 (FIG. 1) without first retrieving a virtual MAC address corresponding to a function accelerator 11 – 14 specified for processing the data. Additionally, Inagaki fails to disclose or suggest a hardwired pipeline operable without executing a program instruction to process data. These teaching deficiencies are illustrated in the discussion above relating to claim 1.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claims 10-12 and 15-16

These claims are patentable at least by virtue of their dependencies from claim 9.

Claim 41

Claim 41 as amended recites processing data with a destination hardwired pipeline circuit without first retrieving a virtual address corresponding to the destination hardwired pipeline circuit and recites various operations performed without executing a program instruction.

In contrast, Inagaki does not disclose or suggest processing data with a pipeline circuit without first retrieving a virtual address corresponding to the pipeline circuit, nor does Inagaki disclose or suggest recited operations without executing a program instruction. These teaching deficiencies are illustrated in the discussion above relating to claim 1.

Claim 42

This claim is patentable at least by virtue of its dependency from claim 41.

Claim 43

Claim 43 recites receiving data without receiving, with the data, information corresponding to a post processing destination of the data, and recites performing various operations without executing a program instruction.

In contrast, Inagaki does not disclose or suggest receiving data without receiving, with the data, information corresponding to a post processing destination of the data, nor does Inagaki disclose or suggest recited operations without executing a program instruction. These teaching deficiencies are illustrated in the discussions above relating to claims 1 and 7.

Claim 83

This claim is patentable at least by virtue of its dependency from claim 43.

Claim 44

Claim 44 as amended recites processing data with a hardwired pipeline without executing a program instruction and without first using a virtual address corresponding to the hardwired pipeline.

In contrast, Inagaki does not disclose or suggest processing data with a hardwired pipeline without first using a virtual address corresponding to the hardwired pipeline, nor does Inagaki disclose or suggest a hardwired pipeline operable without executing a program instruction. These teaching deficiencies are illustrated in the discussion above relating to claim 1.

Claims 45-46 and 49-50

These claims are patentable at least by virtue of their dependencies from claim 44.

Claim 66

Claim 66 as amended recites a hardwired pipeline circuit operable to generate from extracted information an identifier without referencing a virtual address

that identifies a specified pipeline, and recites processing data with a pipeline without executing a program instruction.

For example, referring, *e.g.*, to FIGS. 4 and 5 and paragraphs [97] - [98] of the patent application, a pipeline circuit 80 is operable to generate an identifier that identifies a specified pipeline 74 without referencing a virtual address. The pipeline circuit 80 may receive a message that includes a header and data, and the header may specify the pipeline 74 for processing the data.

In contrast, Inagaki does not disclose or suggest generating an identifier that identifies a specified pipeline without referencing a virtual address. As discussed above in support of patentability of claim 1, and referring, *e.g.*, to FIG. 1 and col. 6, lines 11-20, Inagaki discloses only that a module 6 generates a virtual MAC address to identify a function accelerator (*e.g.*, function accelerator b 11) that is specified by a destination IP address 163 for processing data in an IP packet 134.

Additionally, Inagaki fails to disclose or suggest processing data with a pipeline without executing a program instruction. This teaching deficiency is also illustrated in the discussion above relating to claim 1.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 73

Claim 73 as amended recites an input data handler operable to load data into a memory without first retrieving a virtual address corresponding to an indicated hardwired pipeline, and recites a hardwired pipeline operable to process data without executing a program instruction.

In contrast, Inagaki does not disclose or suggest an input data handler operable to load data into a memory without first retrieving a virtual address corresponding to an indicated hardwired pipeline, nor does Inagaki disclose or suggest a hardwired pipeline operable to process data without executing a program instruction. These teaching deficiencies are illustrated in the discussions above relating to claims 1 and 9.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 76

Claim 76 as amended recites an input data handler operable to load data into a memory without first retrieving a virtual address corresponding to an indicated hardwired pipeline, and recites a hardwired pipeline circuit having components operable without executing a program instruction.

In contrast, Inagaki does not disclose or suggest an input data handler operable to load data into a memory without first retrieving a virtual address corresponding to an indicated hardwired pipeline, nor does Inagaki disclose or suggest the recited components operable without executing a program instruction. These teaching deficiencies are illustrated in the discussions above relating to claims 1 and 9.

Claim 77

This claim is patentable at least by virtue of its dependency from claim 76.

Claim 80

Claim 80 as amended recites generating, without retrieving a virtual address, an identifier that identifies a hardwired pipeline circuit and recites processing data with a hardwired pipeline circuit without executing a program instruction.

In contrast, Inagaki does not disclose or suggest generating, without retrieving a virtual address, an identifier that identifies a hardwired pipeline circuit, nor does Inagaki disclose or suggest processing data with a hardwired pipeline circuit without executing a program instruction. These teaching deficiencies are illustrated in the discussions above relating to claims 66 and 1.

Rejection Of Claims 13-14, 47-48, 67-68, 71-72, 74-75, 78-79, 81-82, and 84-85 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Inagaki In View Of The Examiner's Taking Of Official Notice And Further In View Of U.S. 4,914,653 To Bishop

Claim 13

Claim 13 recites a pipeline interface operable to provide raw data to a hardwired pipeline without using a virtual address, and a hardwired-pipeline circuit comprising components operable without executing a program instruction.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [94] – [102] of the patent application, in an embodiment, regarding providing raw data without using a virtual address, a hardwired-pipeline circuit 80 is operable to provide raw data to a hardwired pipeline 74 without first using a virtual address (see, *e.g.*, paragraph [98]) corresponding to the indicated processing pipeline 74. An input-data handler 120 dissects a message that may have a data payload (*i.e.,* data to be processed by a pipeline 74); pipeline unit address (*e.g.,* physical address for pipeline unit 78, which comprises pipelines 74_1 – 74_n); and a pipeline identifier (*e.g.,* an identifier of one of pipelines 74_1 – 74_n). The data payload is written to a location in DPSRAM 100. A pointer to this location of the data payload and an indication of a destination pipeline (*i.e.,* one of pipelines 74_1 – 74_n) is stored in an input data queue 112. This pipeline indicator relates to a physical address of a pipeline and not a virtual address. When the selected pipeline is ready to process the data payload, the pointer to the data payload location is sent to the selected pipeline, and the selected pipeline retrieves and processes the data payload.

In contrast, Inagaki does not disclose or suggest providing raw data to a hardwired pipeline without using a virtual address. Referring to FIG. 1 and col. 5, line 66 – col. 6, line 35 of Inagaki, a module 6 includes functional accelerators 11 – 14, which are assigned respective virtual MAC addresses b – e. The module 6 receives an IP packet 134 having a destination IP address 163 (FIG. 3), a unit 105 extracts the

destination IP address, and, in response to the extracted IP address, a table 106 provides the virtual MAC address (*e.g.*, address b) of the functional accelerator (*e.g.*, functional accelerator b 11) for processing the data in the IP packet 134. The IP packet 134 (in the form of an Ethernet frame 130) and the virtual MAC address (*e.g.*, address b) are provided to a section 112, which stores the IP packet 134 in the one of the RAMs 150 – 154 (*e.g.*, RAM_b 151) that corresponds to the virtual MAC address (*e.g.*, address b). Subsequently, the module 6 transfers the IP packet 134 from the RAM (*e.g.*, the RAM_b 151) to the one of the function accelerators 11 – 14 (*e.g.*, function accelerator b 11) having the virtual MAC address (*e.g.*, address b) to which the RAM (*e.g.*, the RAM_b 151) corresponds. Consequently, Inagaki's module 6 sends raw data to a functional accelerator if it does not use a virtual MAC address to route the IP packet 134 to the appropriate function accelerator 11 – 14.

Additionally, Inigaki fails to disclose or suggest a hardwired-pipeline circuit comprising the recited components operable without executing a program instruction. This teaching deficiency is illustrated in the discussion above relating to claim 1.

Bishop and the Examiner's Official Notice fail to remedy these teaching deficiencies. Consequently, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not render claim 13 obvious.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 14

Claim 14 as amended recites a pipeline interface operable to provide raw data to a hardwired pipeline without referencing a virtual address, and recites a hardwired pipeline operable to process data without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest providing raw data to a hardwired pipeline without referencing a virtual address, nor does the combination of Inagaki, the Examiner's Official Notice, and Bishop disclose or suggest a hardwired pipeline operable to process

data without executing a program instruction. These teaching deficiencies are illustrated in the discussions above relating to claims 1 and 13.

Claim 47

Claim 47 recites performing certain operations without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest operation without executing a program instruction. This teaching deficiency is illustrated in the discussion above relating to claim 1 and Bishop fails to remedy this teaching deficiency.

Claim 48

Claim 48 recites processing data with a hardwired pipeline without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest processing data with a hardwire pipeline without executing a program instruction. This teaching deficiency is illustrated in the discussion above relating to claim 1 and Bishop fails to remedy this teaching deficiency.

Claim 67

Claim 67 as amended recites generating an identifier that identifies a pipeline without retrieving a virtual address, and processing data with a pipeline without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier that identifies a pipeline without retrieving a virtual address, nor does this combination disclose or suggest processing data with a pipeline without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussion above relating to claims 1 and 66; Bishop fails to remedy these teaching deficiencies.

Claim 68

Claim 68 recites a hardwired pipeline circuit operable to perform operations without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest a hardwired pipeline circuit operable to perform operations without executing a program instruction. This teaching deficiency of Inagaki and the Examiner's Official Notice is illustrated in the discussion above relating to claim 1, and Bishop fails to remedy this teaching deficiency.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 71

Claim 71 as amended recites generating a message header indicating a destination of processed data without using a virtual address, and recites a hardwired pipeline circuit operable to perform operations without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating a message header indicating a destination of processed data without using a virtual address, nor does this combination disclose or suggest a hardwired pipeline circuit operable to perform the recited operations without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussions above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 72

Claim 72 as amended recites generating a message header indicating a destination of processed data without referencing a virtual address, and recites a hardwired pipeline circuit operable to perform instructions without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating a message header indicating a destination of processed data without referencing a virtual address, nor does this combination disclose or suggest a hardwired pipeline circuit operable to perform the recited operations without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notic3 are illustrated in the discussions above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Claim 74

Claim 74 as amended recites a pipeline interface operable to provide retrieved data to a specified hardwired pipeline without using a virtual address, and recites a hardwired pipeline operable to process data without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest a pipeline interface operable to provide retrieved data to a specified hardwired pipeline without using a virtual address, nor does this combination disclose or suggest a hardwired pipeline operable to process data without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussion above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Claim 75

Claim 75 as amended recites a pipeline interface operable to provide retrieved data to a specified hardwired pipeline without referencing a virtual address,

and recites a hardwired pipeline circuit operable to perform actions without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest a pipeline interface operable to provide retrieved data to a specified hardwired pipeline without referencing a virtual address, nor does this combination disclose or suggest a hardwired pipeline circuit operable to perform actions without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussion above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Claim 78

Claim 78 as amended recites a pipeline interface operable to provide data to a hardwired pipeline without using a virtual address and recites a hardwired pipeline circuit operable to perform actions without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest a pipeline interface operable to provide data to a hardwired pipeline without using a virtual address, nor does this combination disclose or suggest a hardwired pipeline circuit operable to perform the recited actions without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussion above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Claim 79

Claim 79 as amended recites a pipeline interface operable to provide data to a hardwired pipeline without referencing a virtual address, and recites a hardwired pipeline circuit operable to perform actions without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest a pipeline interface operable to provide data to a hardwired pipeline without referencing a virtual address, nor does this combination

disclose or suggest a hardwired pipeline circuit operable to perform the recited actions without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussion above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Claim 81

Claim 81 as amended recites generating an identifier that identifies a hardwired pipeline circuit without using a virtual address, and recites processing data with a hardwired pipeline circuit without executing a program instruction.

In contrast, Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier that identifies a hardwired pipeline circuit without using a virtual address, nor does Inagaki, Examiner's Official Notice, and Bishop disclose or suggest processing data with a hardwired pipeline circuit without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussions above relating to claims 1 and 66; and Bishop fails to remedy these teaching deficiencies.

Claim 82

Claim 82 recites a method involving a hardwired pipeline circuit that includes steps which occur without executing a program instruction. For example, processing data with a hardwired pipeline circuit and loading the processed data into a memory.

In contrast, Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest operation without executing a program instruction. This teaching deficiency of Inagaki and the Examiner's Official Notice is illustrated in the discussion above relating to claim 1; and Bishop fails to remedy this teaching deficiency.

Claim 84

Claim 84 recites receiving data without receiving, with the data, information corresponding a post processing destination of the data, and recites processing data with a hardwired pipeline circuit without executing a program instruction.

In contrast, Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest receiving data without receiving, with the data, information corresponding a post processing destination of the data, nor does Inagaki, the Examiner's Official Notice, and Bishop disclose or suggest processing data with a hardwired pipeline circuit without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussions above relating to claim 1 and 7; and Bishop fails to remedy these teaching deficiencies.

Claim 85

Claim 85 recites receiving data without receiving, with the data, information corresponding a post processing destination of the data, and recites processing data with a hardwired pipeline circuit without executing a program instruction.

In contrast, Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest receiving data without receiving, with the data, information corresponding a post processing destination of the data, nor does Inagaki, the Examiner's Official Notice, and Bishop disclose or suggest processing data with a hardwired pipeline circuit without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussions above relating to claim 1 and 7; and Bishop fails to remedy these teaching deficiencies.

Conclusion

In view of the foregoing, the application is believed to be in a condition for allowance. The Examiner is encouraged to contact the undersigned via telephone if a conference would expedite prosecution of this matter.

The filing of this document constitutes a request for any needed extension of time. The Commissioner is hereby authorized to charge any deficiency of fees submitted herewith, or credit any overpayment, to Deposit Account No. 07-1897.

Dated the 7th day of June, 2010

Respectfully submitted,

/Dylan O. Adams/

Dylan O. Adams
Registration No. 56,289

Customer No. 00996

Graybeal Jackson Haley LLP
400 - 108th Avenue NE, Suite 700
Bellevue, Washington 98004
Telephone: 425.455.5575
Facsimile: 425.455.1046